REMARKS

Claims 1-3 and 5-10 are all the claims pending in the application. Claims 1-3, 5-7, and 9-10 are rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Hanselmann, "Real-Time Simulation Replaces Test Drives", Test and Measurement World, February 15, 1996, pages 35-36, 38, 40. Claim 8 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Hanselmann in view of Turner (U.S. Patent No. 6,269,020).

§ 102(b) Rejections (Hanselmann) – Claims 1-3, 5-7, 9, and 10

Claims 1-3, 5-7, 9, and 10 are rejected for the reasons set forth on pages 2-5 of the present Office Action.

With respect to independent claim 1, Applicant submits that Hanselmann does not disclose or suggest at least, "sending input signals to said unit and receiving low output signals from said unit in response to said input simulation signals by at least one microprocessor," "receiving fast output signals in response to said input simulation signals by at least one programmable logic circuit," and "processing the fast output signals by the at least one logic circuit to generate parameters values at a first frequency," as recited in amended claim 1.[1] At page 36, column 1, Hanselmann discloses "the gray box on the left contains the real-time hardware for the test bench multiple digital signal processor (DSPs), I/O boards and interfacing circuitry" and "the real-time hardware handles all closed-loop computing, which has to meat stringent time requirements". Applicant submits these sentences disclose that a gray box

[1] Support for these amendments to claim 1 can be found at page 7, line 17 to page 8, line 8 of specification and in figure 1, for example. Also, Applicant respectfully requests that the Examiner enter these claim amendments as the claimed invention has already been substantially considered by the Examiner.

contains hardware enabling closed-loop computing in real-time. However, these sentences do not disclose how a simulator operates to obtain a computing in real-time. In particular, these passages do not disclose that one of the multiple DSPs (i.e. the DDS or the parallel processing DSP) receives fast output signals from the unit under test.

As described at page 36, column 3, paragraph 2, Hanselmann discloses that "the direct digital synthesis or DDS is a digital-to-analog converter generating wheel speed signals that replaces those from a magnetic detector of the Audi's car. These signals are sinusoids with both frequency and amplitude proportional to wheel speeds." So, the digital-to-analog converter DDS produces analog signals for the unit under test, but it does not receive and process fast output signals received from the unit under test.

Further, as described at page 36, column 2, last paragraph of Hanselmann, the multiprocessor DSP system contains a "Master DSP" and a "parallel processing DSP". So, the "parallel processing DSP" is a coprocessor which allows processing the simulation in itself in real-time by computing one part of the computing of the Master DSP. The parallel processing DSP does not process the fast output signals from the unit under test.

According to an exemplary embodiment of the present invention, since the microprocessor 14 does not have the capacity for processing enough quickly the fast output signals, the simulator can comprise a logic circuit 18 adapted to receive, process and store in a memory 19 the result of the output signals processed by the logic circuit 18. The microprocessor 14 is able to access the memory 19 at its own frequency to take the result already processed by the logic circuit 18.

Hanselmann describes a simulator which comprises several microprocessors operating in real-time. However, it does not disclose that a logic circuit (DDS, parallel processing DSP) processes fast output signals and stores them in a memory and that a microprocessor 14 (Master DSP) processes low signals and accesses the processed fast output signals in the memory 19 at its own frequency.

Yet further, in response to the Examiner's arguments in paragraph 8.3 of the Office Action, at page 36, column 3, paragraph 3, Hanselmann discloses that "the DSP generates signals much faster than the vehicle simulation." At page 36, column 3, paragraph 1, Hanselmann discloses that the duration of the vehicle simulation is smaller than 1 microsecond. Hanselmann does not disclose that the duration of the vehicle simulation corresponds to the time between two accesses of the microprocessor 14 (Master DSP) to the memory of the logic circuit 18 (DDS, parallel processing DSP).

At least based on the explanation above, Applicant submits that Hanselmann does not satisfy at least the above-quoted features of claim 1, and, thus, does not anticipate claim 1.

With respect to independent claim 5, Applicant amends this claim and submits that claim 5 is patentable at least based on reasons similar to those set forth above with respect to claim 1. Further, with respect to claim 5, and in response to the Examiner's arguments in paragraph 4-4 of the Office Action, at page 38, column 2, last paragraph, Hanselmann describes "a computing environment like MATLAB which can be useful when you use it with DSPs in real-time applications. The Audi test bench is connected to the DSP through M (a software tool that lets MATLAB interface directly with the DSP) and MTRACE (a support tool that records time histories on the DSP and uploads them to the MATLAB workspace)". In other words, the

software MATLAB is connected between the electronic unit (test bench) and the DSP and accesses the data stored in the DSP. Hanselmann does not disclose if this DSP is the Master DSP, the DSP of the DDS or the parallel processing DSP. This paragraph does not disclose that the Master DSP accesses the parameter values stored in the memory 19 of the logic circuit 18 (DDS, parallel processing DSP). Since the microprocessor 14 (Master DSP) does not access the parameter values in the memory 19, the access frequency of this microprocessor can not be compared to, and should not be confused with, the frequency of generation of the parameter values. At least based on the foregoing, Applicant maintains that Hanselmann does not anticipate claim 5.

Applicant submits that claims 2, 3, 6, 7, 9, and 10 are allowable at least by virtue of their respective dependencies from independent claims 1 and 5.

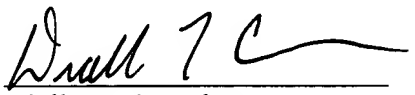
§ 103(a) Rejection (Hanselmann / Turner) – Claim 8

Applicant submits that dependent claim 8 is allowable at least by virtue of its dependency from independent claim 5. Turner does not make up for the deficiencies of Hanselmann.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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